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application INFO available

UCC1806
UCC2806
UCC3806

Low Power, Dual Output, Current Mode PWM Controller

FEATURES

- BiCMOS Version of UC1846 Families
- 1.4mA Maximum Operating Current
- 100µA Maximum Startup Current
- 1.0A Peak Output Current
- 125nsec Circuit Delay
- Easier Parallelability
- Improved Benefits of Current Mode Control

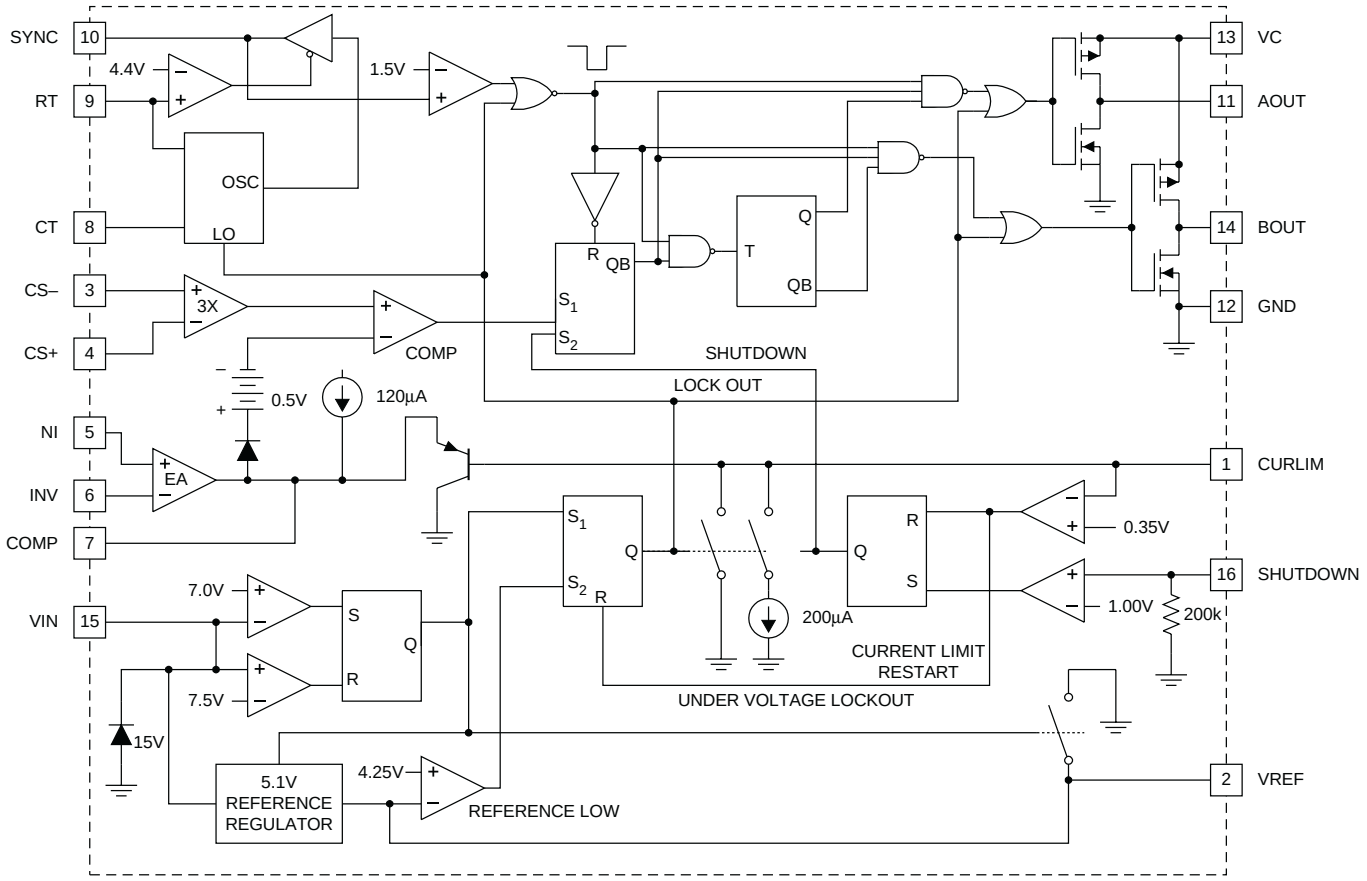
DESCRIPTION

The UCC1806 family of BiCMOS PWM controllers offers exceptionally improved performance with a familiar architecture. With the same block diagram and pinout of the popular UC1846 series, the UCC1806 line features increased switching frequency capability while greatly reducing the bias current used within the device. With a typical startup current of 50µA and a well defined voltage threshold for turn-on, these devices are favored for applications ranging from off-line power supplies to battery operated portable equipment. Dual high current, FET driving outputs and a fast current sense loop further enhance device versatility.

All the benefits of current mode control including simpler loop closing, voltage feed-forward, parallelability with current sharing, pulse-by-pulse current limiting, and push-pull symmetry correction are readily achievable with the UCC1806 series.

(continued)

BLOCK DIAGRAM



Pin numbers refer to DIL-16 package.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, Low Impedance (Pin 15) . . . . . +15V
Supply Current, High Impedance (Pin 15) . . . . . +25mA
Output Supply Voltage (Pin 13) . . . . . +18V
Output Current, Continuous Source or Sink . . . . . ±200mA
Output Current, Gate Drive . . . . . ±500mA
Analog Input Voltage (Pin 3, 4, 5, 6, 16) . . –0.3V to +V_{IN} +0.3V
Sync Output Current (Pin 10) . . . . . ±30mA
Error Amplifier Output Current (Pin 7) . +10mA/– (Self Limiting)
Power Dissipation at T_A = 25°C (Note 3) 1000mW
Power Dissipation at T_C = 25°C (Note 3) 2000mW
Storage Temperature Range . . . . . 65°C to +150°C
Lead Temperature (soldering, 10 seconds) . . . . . +300°C

Note 1. All voltages are with respect to Ground, Pin 12.

Note 2. Currents are positive into, negative out of the specified terminal.

Note 3. Consult packaging section of databook for thermal limitations and considerations of package.

Note 4. Pin numbers refer to DIL-16 package.

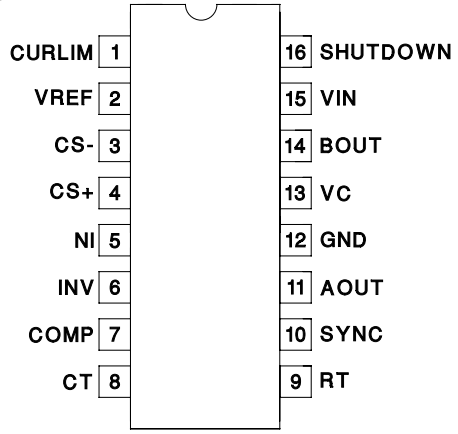
DESCRIPTION (continued)

These devices are available with multiple package options for both through-hole and surface mount applications; and in commercial, industrial, and military temperature ranges. Contact factory for availability.

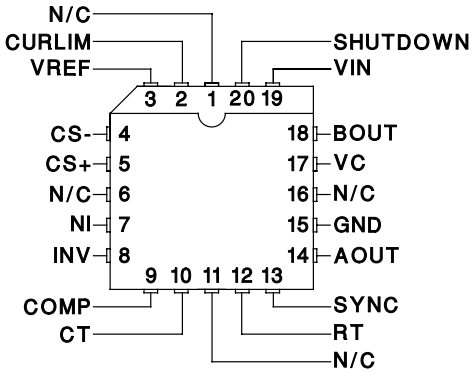
The UCC1806 is specified for operation from –55°C to +125°C, the UCC2806 is specified for operation from –40°C to +85°C, and the UCC3806 is specified for operation from 0°C to +70°C. The part is available in DIP and SOIC packages.

CONNECTION DIAGRAMS

DIL-16 (Top View)
J or N, DW PACKAGE



PLCC-20, LCC-20 (Top View)
Q, L PACKAGE



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications hold for T_A = –55°C to +125°C for the UCC1806, –40°C to +85°C for the UCC2806, and 0°C to +70°C for the UCC3806; V_{IN} = 12V, R_T = 33k, C_T = 330pF, C_{BYPASS} on V_{REF} = 0.01µF, T_A = T_J.

PARAMETER	TEST CONDITION	UCC1806 / UCC2806			UCC3806			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage	T_J = 25°C, I_O = 0.2mA	5.02	5.10	5.17	5.00	5.10	5.20	V
Load Regulation	0.2mA < I_O < 5mA		3	25		3	25	mV
Total Output Variation	Line, Load, Temperature (Note 7)	–150		150	–150		150	mV
Output Noise Voltage	10Hz ≤ f ≤ 10kHz, T_J = 25°C (Note 5)		70			70		µV
Long Term Stability	T_A = 125°C, 1000 Hours (Note 5)		5	25		5	25	mV
Output Short Circuit		–10		–30	–10		–30	mA

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications hold for T_A = –55°C to +125°C for the UCC1806, –40°C to +85°C for the UCC2806, and 0°C to +70°C for the UCC3806; V_{IN} = 12V, R_T = 33k, C_T = 330pF, C_{BYPASS} on V_{REF} = 0.01µF, $T_A = T_J$.

PARAMETER	TEST CONDITION	UCC1806 / UCC2806			UCC3806			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Oscillator Section								
Initial Accuracy	T_J = 25°C	42	47	52	42	47	52	kHz
Temperature Stability	$T_{MIN} < T_A < T_{MAX}$ (Note 5)		2			2		%
Amplitude			2.35			2.35		V
SYNC Delay to Outputs	Pin 8 = 0V, Pin 9 = V_{REF}, V_{SYNC} = 0.8V to 2.0V		50	125		50	100	ns
Discharge Current	T_J = 25°C, V_{PIN} 8 = 2.0V		2			2		mA
SYNC, V_{OL}	I_{OUT} = +1mA			0.4			0.4	V
SYNC, V_{OH}	I_{OUT} = –4mA	2.4			2.4			V
SYNC, V_{IL}	Pin 8 = 0V, Pin 9 = V_{REF}			0.8			0.8	V
SYNC, V_{IH}	Pin 8 = 0V, Pin 9 = V_{REF}	2.0			2.0			V
SYNC Input Current		–1		+1	–1		+1	µA
Error Amplifier Section								
Input Offset Voltage				5			10	mV
Input Bias Current				–1			–1	µA
Input Offset Current				500			500	nA
Common Mode Range		0		V_{IN}-2	0		V_{IN}–2	V
Open Loop Gain	V_O = 1.0 to 4.0	80	100		80	100		dB
Unity Gain Bandwidth		1			1			MHz
Output Sink Current	V_{ID} < –20mV, $V_{PIN\ 7}$ = 1.0V	1			1			mA
Output Source Current	V_{ID} < 20mV, $V_{PIN\ 7}$ = 3.0V	–80	–120		–80	–120		µA
Output High Level	V_{ID} = –50mV	4.5			4.5			V
Output Low Level	V_{ID} = –50mV			0.5			0.5	V
Current Sense Amplifier Section								
Amplifier Gain	$V_{PIN\ 3}$ = 0V, $V_{PIN\ 1}$ = V_{REF} (Notes 3,4)	2.75	3	3.35	2.75	3	3.35	V/V
Maximum Differential Input Signal ($V_{PIN\ 4}$ - $V_{PIN\ 3}$)	$V_{PIN\ 1}$ = V_{REF}, $V_{PIN\ 5}$ = V_{REF}, $V_{PIN\ 6}$ = 0V	1.1			1.1			V
Input Offset Voltage	$V_{PIN\ 1}$ = 0.5V, $V_{PIN\ 7}$ = OPEN		10	30		10	50	mV
CMRR	V_{CM} = 0 to V_{IN} – 3.5	60			60			dB
PSRR		56			56			dB
Input Bias Current	$V_{PIN\ 1}$ = 0.5V, PIN 7 OPEN (Note 3)			–1			–1	µA
Input Offset Current	$V_{PIN\ 1}$ = 0.5V, PIN 7 OPEN (Note 3)			1			1	µA
Delay to Outputs	$V_{PIN\ 5}$ = V_{REF}, PIN 6 = 0, PIN 1 = 2.75V, PIN 4 – PIN 3 = 0 to 1.5V step (Note 6)		125	175		125	175	ns
Current Limit Adjust Section								
Current Limit Offset	$V_{PIN\ 3}$ = 0, $V_{PIN\ 4}$ = 0, PIN 7 = open	0.40	0.50	0.60	0.40	0.50	0.60	V
Input Bias Current				1			1	µA
Minimum Latching Current		300	200		300	200		µA
Maximum Non-Latching Current			200	80		200	80	µA
Shutdown Terminal Section								
Threshold Voltage		0.94	1.00	1.06	0.9	1.0	1.1	V
Input Voltage Range		0		V_{IN}	0		V_{IN}	V
Delay to Outputs	$V_{PIN\ 16}$ = 0 to 1.3V		75	150		75	150	ns

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications hold for T_A = –55°C to +125°C for the UCC1806, –40°C to +85°C for the UCC2806, and 0°C to +70°C for the UCC3806; V_{IN} = 12V, R_T = 33k, C_T = 330pF, C_{BYPASS} on V_{REF} = 0.01µF, $T_A = T_J$.

PARAMETER	TEST CONDITION	UCC1806 / UCC2806			UCC3806			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Output Section								
Output Supply Voltage		2.5		15	2.5		15	V
Output Low Level	I_{SINK} = 20mA		100	300		100	200	mV
	I_{SINK} = 100mA		0.40	1.1		0.40	1.1	V
Output High Level	I_{SOURCE} = –20mA	11.6	11.9		11.6	11.9		V
	I_{SOURCE} = –100mA	11	11.6		11	11.6		V
Rise Time	T_J = 25°C, C_{LOAD} = 1000pF		35	65		35	65	ns
Fall Time	T_J = 25°C, C_{LOAD} = 1000pF		35	65		35	65	ns
Under Voltage Lockout Section								
Startup Current	V_{IN} < Start Threshold		50	100		50	100	µA
Operating Supply Current			1	1.4		1	1.4	mA
V_{IN} Shunt Voltage	I_{VIN} = 10mA	15		17.5	15		17.5	V
Startup Threshold		6.5	7.5	8	6.5	7.5	8	V
Threshold Hysteresis			0.75			0.75		V

Note 1: All voltages are with respect to Ground, Pin 12.

Note 2: Currents are positive into, negative out of the specified terminal.

Note 3: Parameters measured at trip point of latch with $V_{PIN\ 5} = V_{REF}$, $V_{PIN\ 6}$ = 0V.

Note 4: Amplifier gain defined as: G = delta change at Pin 7/delta change forced at Pin 4 delta voltage at Pin 4 = 0 to 1V.

Note 5: Guaranteed by design. Not 100% tested in production.

Note 6: Current Sense Amp output is slew rate limited to provide noise immunity.

Note 7: Line Range = 10V to 15V, Load Range = 0.2mA to 5mA.

PIN DESCRIPTIONS

AOUT and BOUT: AOUT and BOUT provide alternating high current gate drive for the external MOSFETs. Duty cycle can be varied from 0 to 50% where minimum dead time is a function of CT. Both outputs use MOS transistor switches with inherent anti-parallel body diodes to clamp voltage swings to the supply rails, allowing operation without the use of clamp diodes.

COMP: COMP is the output of the error amplifier and the input of the PWM comparator. The error amplifier is a low output impedance, 2MHz operational amplifier which allows sinking or sourcing of current at the COMP pin. The error amplifier is internally current limited, so that zero duty cycle can be commanded by externally forcing COMP to GND.

CS–: CS- is the inverting input of the 3X, differential current sense amplifier.

CS+: CS+ is the non-inverting input of the 3X, differential current sense amplifier.

CT: CT is the oscillator timing capacitor connection point, which is charged by the current set by RT. CT is discharged to GND through a 2.6mA current sink. This causes a linear discharge of CT to zero volts which then initiates the next switching cycle. Dead time occurs during the discharge of CT, forcing AOUT and BOUT low. Switching frequency (fs) and dead time (td) are approximated by:

$$fs = \frac{1}{2 \bullet RT \bullet CT + td} \text{ and } td = 961 \bullet CT$$

CURLIM: CURLIM programs the primary current limit threshold and determines whether the device will latch off or retry after an overcurrent condition. When a shutdown signal is generated, a 200µA current source to ground pulls down on CURLIM. If the voltage on the pin remains above 350mV the device remains latched and the power must be cycled to restart. If the voltage on the pin falls below 350mV, the device attempts a restart. The voltage threshold is typically set by a resistor divider from

PIN DESCRIPTIONS (continued)

V_{REF} to ground. To calculate the current limit adjust voltage threshold the following equations can be used;

Current Limit Adjust Latching Mode Voltage:

$$V = \frac{V_{REF} - (R1 \bullet 300\,\mu A)}{1 + \frac{R1}{R2}} > 350mV$$

Current Limit Adjust Non-Latching Mode Voltage:

$$V = \frac{V_{REF} - (R1 \bullet 80\,\mu A)}{1 + \frac{R1}{R2}} > 350mV$$

where R1 is the resistance from the V_{REF} to CURLIM and R2 is the resistance from CURLIM to GND.

GND: GND is the reference ground and power ground for all functions of this part. Bypass and timing capacitors should be connected as close as possible to GND.

INV: INV is the inverting input of the error amplifier and has a common mode range from 0V to V_{IN} –2V.

NI: NI is the non-inverting input of the error amplifier and has a common mode range from 0V to V_{IN} –2V.

RT: RT is the connection point for the oscillator timing resistor. It has a low impedance input and is nominally at 1.25V. The current through RT is mirrored to the timing capacitor pin, CT. This causes a linear charging of CT from 0V to 2.35V. Note that the current mirror is limited to a maximum of 100µA so RT must be greater than 12.5k.

SHUTDOWN: The SHUTDOWN pin is provided for enhanced protection. When SHUTDOWN is driven above 1V, AOUT and BOUT are forced low.

SYNC: SYNC is a bi-directional pin, allowing or providing external synchronization with TTL compatible thresholds. In a typical application RT is connected through a timing resistor to GND which allows the internal oscillator to free run. In this mode SYNC outputs a TTL compatible pulse during the oscillator dead time (when CT is being discharged). If RT is forced above 4.4V, SYNC acts as an input with TTL compatible thresholds and the internal oscillator is disabled. When SYNC is high, greater than 2V the outputs are held active low. When SYNC returns low, the outputs may be high until the on-time is terminated by the normal peak current signal, a fault seen at SHUTDOWN or the next high assertion of SYNC. Multiple UCC3806s can be synchronized by a single master UCC3806 or external clock.

VC: VC is the input supply connection for the FET drive outputs and has an input range of 2.5V to 15V. VC should be capacitively bypassed for proper operation.

V_{IN}: V_{IN} is the input supply connection for this device. The UCC1806 has a maximum startup threshold of 8V and internally limited by means of a 15V shunt regulator. The shunted supply current must be limited to 2.5mA. For proper operation, VIN must be bypassed to GND with at least a 0.01µF ceramic capacitor.

V_{REF}: V_{REF} is a 5.1V ±1% trimmed reference output with a 5mA maximum available current. V_{REF} must be bypassed to GND with at least a 0.1µF ceramic capacitor for proper operation.

TYPICAL CHARACTERISTICS

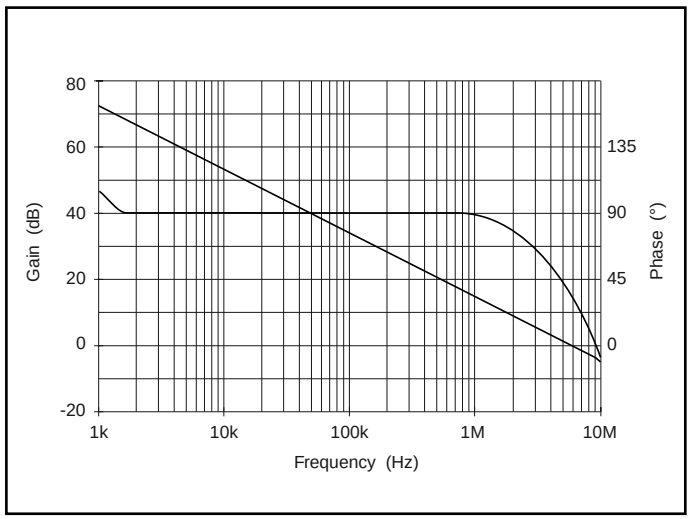


Figure 1. Error amplifier gain and phase response.

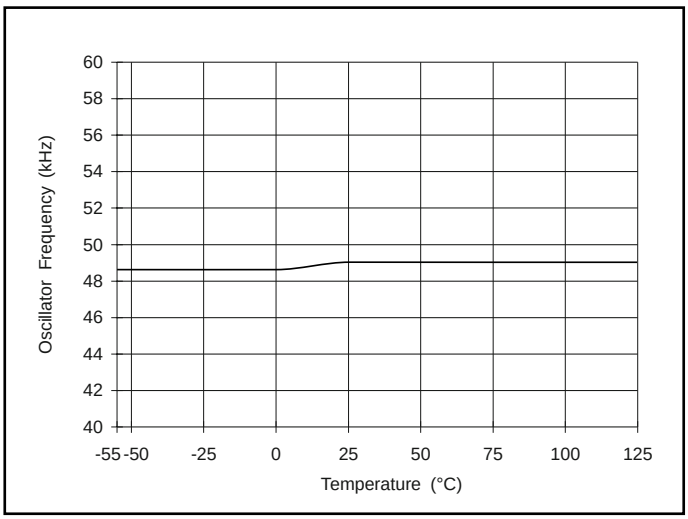


Figure 2. Oscillator frequency vs. temperature.

TYPICAL CHARACTERISTICS (continued)

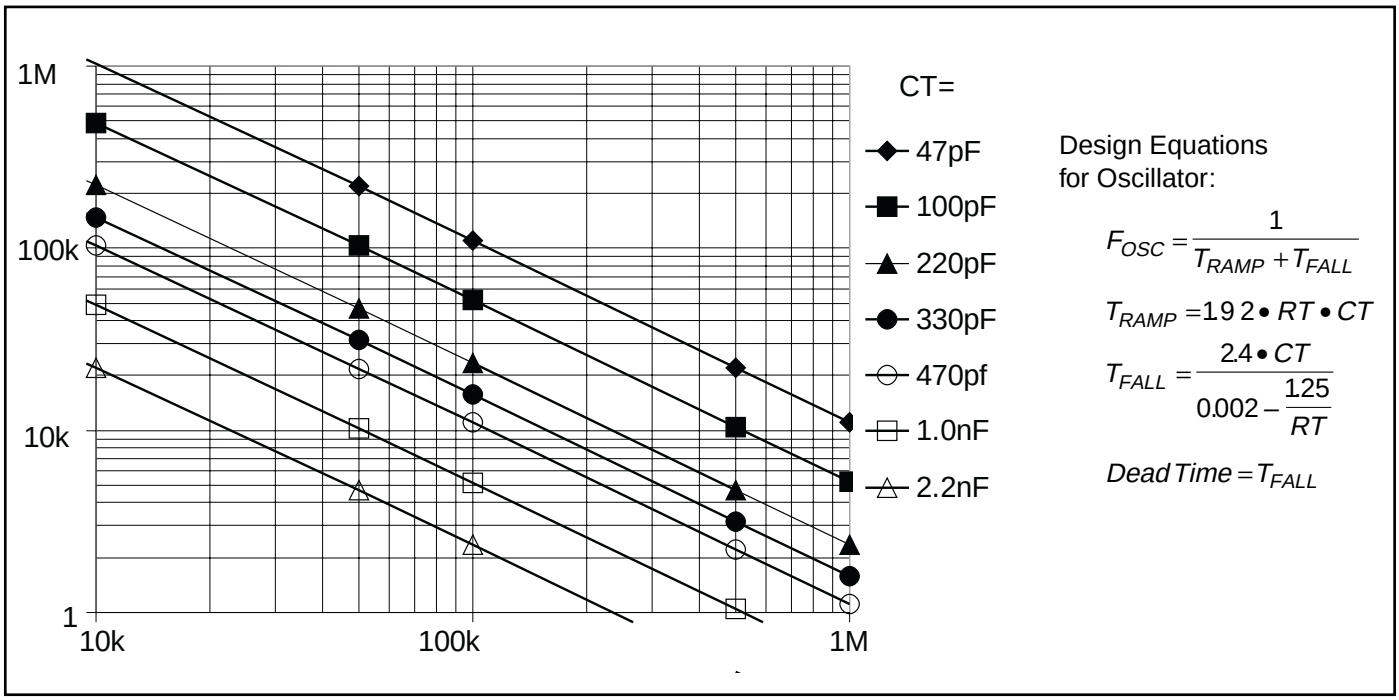


Figure 3. Oscillator frequency vs. RT and CT.

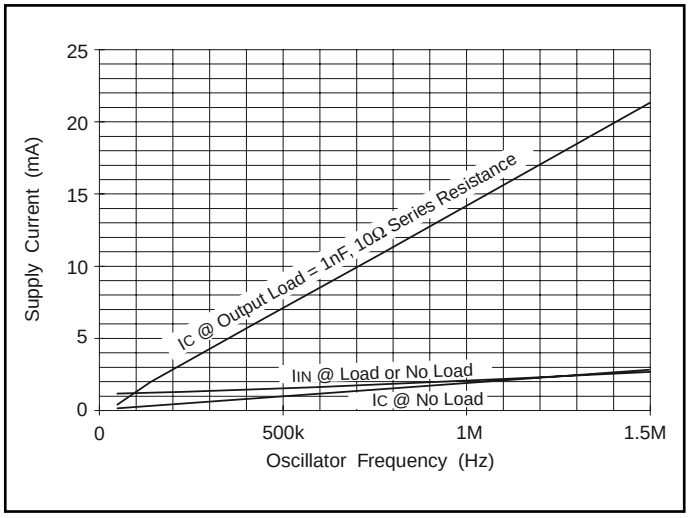


Figure 4. Supply current vs. oscillator frequency.

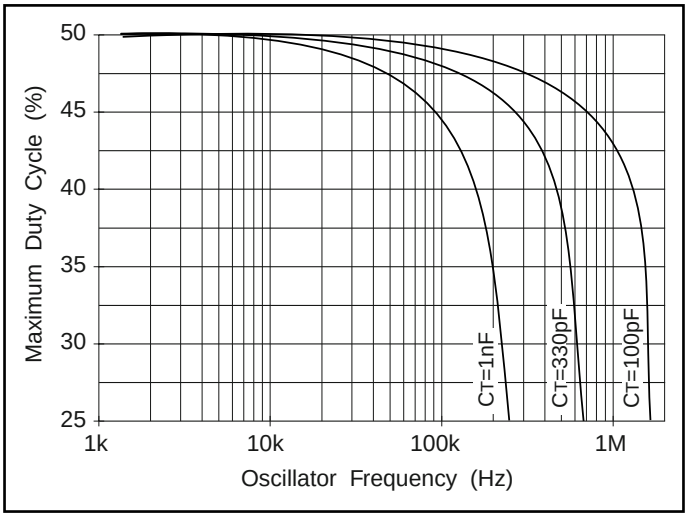
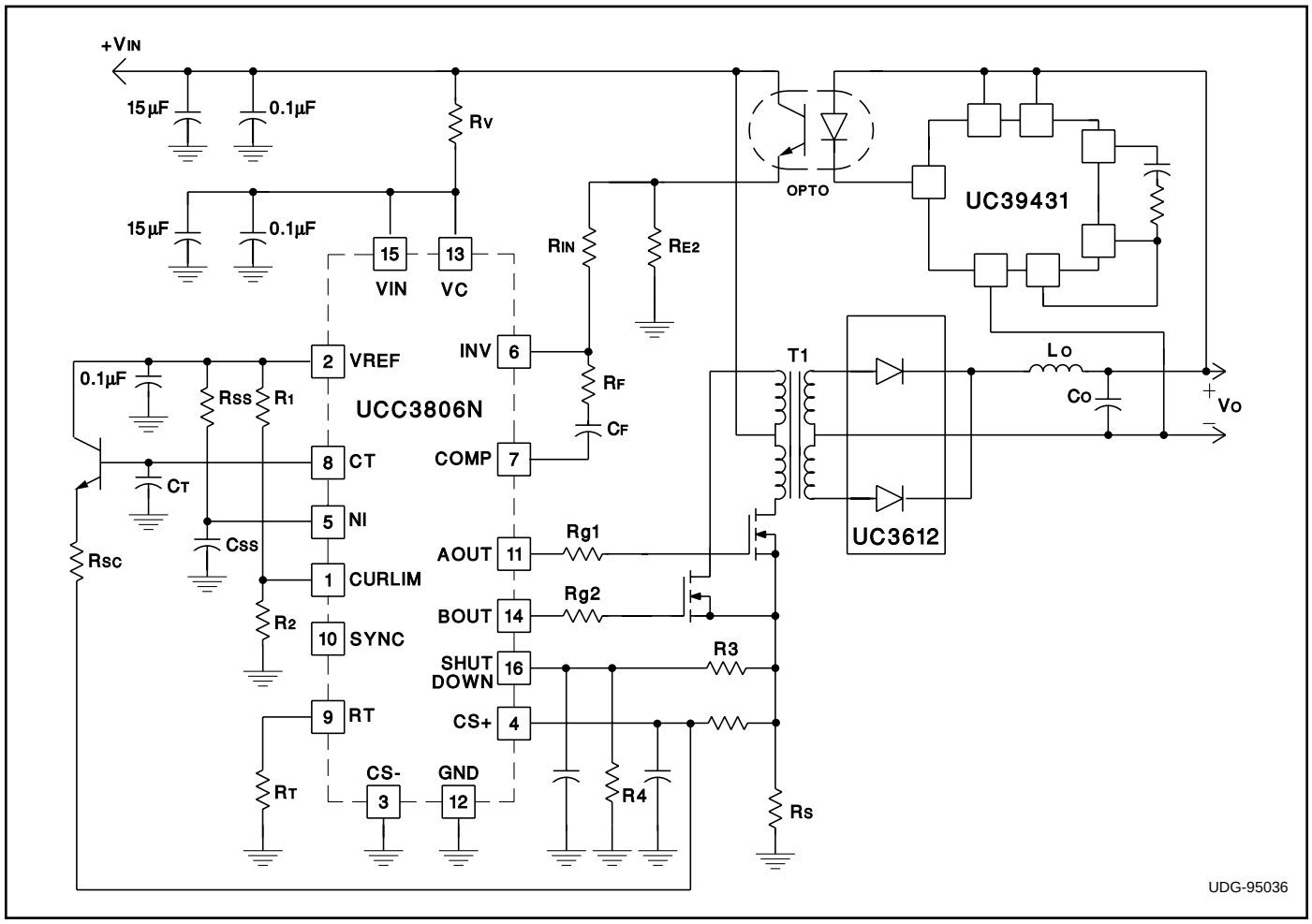


Figure 5. Maximum duty cycle vs. frequency.

TYPICAL APPLICATION



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